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A DEVICE THAT PROVIDES THE FUNCTIONALITY OF DUAL-PORTED MEMORY USING SINGLE-PORTED MEMORY FOR MULTIPLE CLOCK DOMAINS

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A DEVICE THAT PROVIDES THE FUNCTIONALITY OF DUAL-PORTED MEMORY USING SINGLE-PORTED MEMORY FOR MULTIPLE CLOCK DOMAINS

Background Of The Invention

Related Applications

The present application is related to and claims priority from and herein incorporates by reference the US provisional patent application serial number 60/445,872, entitled "Dual-Port Memory Using Single Port Memory for Multiple Clock Domain", by inventor, S. Babar Raza, filed on February 7, 2003. This present application is related to and herein incorporates by reference the US provisional patent application serial number 60/436,303, entitled "A Logic for Implementing a Dual Clock Domain Read Access with Predictable Timing for Bi-directional I/Os," by the same inventor, filed on December 31, 2002. The present application is related to and herein incorporates by reference the US non-provisional patent application serial number xx/xxx,xxx, entitled "Logic for Implementing a Dual Clock Domain Read Access with Predictable Timing for Bi-Directional Inputs/Outputs" by the same inventor, filed on December 24, 2003.

Field of the Invention

Embodiments of the present invention relate to the field of electronic circuitry. More specifically, embodiments of the present invention relate to memory where dual port operation can be emulated for applications operating according to multiple clock domains using a single port memory.

Related Art

Random access memory cells or RAMs have become increasingly more popular due in part to the attractive costs of these devices. Many conventional RAM cells are ordinarily only addressable from a single port. In such a memory apparatus,

the input of a binary address causes a single select line or coincidence of two select lines, such as a row select line and a column select line, to cause the addressed cell to be selected. Upon selection of a cell, data may then be sensed from or written into the selected storage cell on one or two bit sense lines. Alternatively, in some RAM cells, a single selection line causes the particular cell to be selected, and other selection circuitry activated by the same address causes the bit-sense lines to be selected. However, there are generally no options for addressing, sensing, and writing. The same selection lines and the same bit sense lines are always utilized to access, write to, and sense a particular location. Consequently, a single port RAM memory device cannot be simultaneously addressed and accessed from separate sources, thus, limiting access speed at which the RAM memory may be accessed.

However, certain applications require higher memory access speeds than what a single port RAM memory device can provide. Examples of such high speed applications may be graphic related memory systems such as those used in computer display systems, data transfer and buffering devices used in high speed communications systems, and memory systems used in communication with arithmetic logic units. For such applications, multi-ported random access memory devices have been developed to provide higher access speeds and increased accessibility to the memory contents of the random access memory unit. One example of a multi-ported memory device is a dual-ported RAM cell accessible simultaneously by two independent entities. In digital integrated circuits (ICs), this implies a dual-ported memory cell that can be accessed at the same time through two different ports. Each port utilizes independent sets of addresses and control lines to access the memory array using more than one clock (referred to hereinafter as "multiple clock domains") to synchronize the data from the address and control lines.

FIG. 1 depicts a block diagram of dual-ported memory. The device 100 depicted in FIG. 1, includes a dual-ported memory 130 with two ports (110, 120). Therefore, one entity can read and/or write data to dual-ported memory 130 using port 110 while another entity may simultaneously read and/or write data to dual-ported memory 130 using port 120. Each port supports a respective address bus (112, 122) and respective buses (114, 124) for data input and output (as well as port clock lines (116, 126) for controlling the synchronization of reading and/or writing data to and/or from the port data buses (114, 124). Since, device 100 has two clock lines (116, 126) for synchronizing data input and/or output, device 100 can support "multiple clock domains," enabling the processing of large amounts of data very quickly and efficiently.

Although the dual-ported memory 100 provides an effective solution for dual-port functionality, it results in large circuit designs and high development costs. For each new generation of fabrication process technology, a new dual port cell must be designed and tested, leading to additional development costs. For the same density, a dual-ported memory 100 is approximately twice the size of a single-ported memory. As performance requirements rise, more advanced technology may be required to implement a dual-ported memory than to implement a single-ported memory, rendering the conventional dual-ported memory less attractive.

FIG. 2 depicts a block diagram of another type of dual-ported memory. As depicted in FIG. 2, the dual-ported memory 200 has a port clock domain 212, which is associated with a clock signal that is received on port clock line 224, and a memory clock domain 214, which is associated with a clock signal that is communicated on clock line 226. A clock domain boundary 262 separates the port clock domain 212 from the memory clock domain 214.

Data is received by the dual-ported memory 200 at the port data bus 222. The clock signal received on port clock line 224 is used for synchronizing data received on port data bus 222. The data that is received on port data bus 222 crosses the clock domain boundary 262 through a data first-in-first-out (FIFO) 230, which is used to synchronize the data received on port address bus 222 with the memory clock domain 214.

The data is communicated from the data FIFO 230 to a memory controller 240 along bus 232. The address logic 242 of memory controller 240 generates an address that the data may be stored at in the single clock domain memory 250. Memory controller 240 communicates the data to the single clock domain memory 250, along with the generated address, and a clock signal along the respective buses (244, 246) and control line (226). Single clock domain memory 250 stores the data at the address that address logic 242 generated.

Although device 200 is size efficient it can only be used for uni-directional data flow and is most suitable for sequential data processing.

SUMMARY OF THE INVENTION

It would be advantageous to provide memory that is small and cost effective to manufacture but that has the functionality of dual-ported memory.

Accordingly, embodiments of the present invention provide the functionality of a dual-ported memory using single-ported memory for multiple clock domain applications.

Embodiments of the present invention are directed to a device that improves upon the conventional device, where size (and therefore cost), is important and where the ability to interface with multiple clock domains and perform random accesses and bi-directional accesses is important. In one embodiment, memory device comprises two or more port synchronization logic devices, a port multiplexing logic, and a single-ported memory core. The port synchronization logic devices synchronize information communicated between ports associated with the port synchronization logic devices and the single-ported memory core by synchronizing the information between port clocks and a core clock. The two ports and the core clock can operate at different frequencies. Typically, the core frequency is twice that of the fastest port frequency.

More specifically, in one embodiment the port synchronization logic devices include FIFOs for synchronizing the information communicated between the ports and the single-ported memory core. For example, the port synchronization logic devices may include read data control FIFOs, write data and control FIFOs, and address FIFOs

In another embodiment, the port synchronization logic devices include multiplexers which can be used for bypassing the synchronization of the information

communicated between the ports and the single-ported memory core in the event that the port clocks and the core clock are derived from the same clock source circuit.

In one embodiment, the port multiplexing logic acts as a time division multiplexer (TDM) for information communicated between the port synchronization logic devices and the single-ported memory core.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 depicts a block diagram of dual-ported memory of the conventional art.

FIG. 2 depicts a block diagram of another type of dual-ported memory of the conventional art.

FIG. 3 depicts a memory circuit device that has the functionality of a dual-ported memory but which is constructed from single-ported memory according to one embodiment of the present invention.

FIG. 4 depicts a port synchronization logic device according to one embodiment of the present invention.

FIG. 5 depicts another port synchronization logic device according to another embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the preferred embodiments of the present invention, device is described that provides the functionality of a dual-ported memory using a single-ported memory for multiple clock domains, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

FIG. 3 depicts a memory circuit device that has the functionality of a dual-ported memory but which is constructed from single-ported memory according to one embodiment of the present invention. As depicted in FIG. 3, memory circuit device 300 includes two port synchronization logic devices (330, 340), a port multiplexing logic 370, a controller 390, and a single-ported memory core 380.

According to one embodiment, both of the port synchronization logic devices (330, 340) communicate with respective ports (310, 320) which may operate at different and independent frequencies. For example, each of the respective ports (310, 320) may include respective buses (312, 322, 314, 324), such as a port data

bus (312, 322) for receiving and outputting data, as well as a port address bus (314, 322) for receiving an address that data received on a port data bus (312, 322) may be ultimately stored at in the single-ported memory core 380.

According to another embodiment, device 300 has a port multiplexing logic 370 so that device 300 can operate with multiple ports (330, 340). According to one embodiment, port multiplexing logic 370 acts as a time division multiplexer (TDM) for data and addresses communicated between the port synchronization logic devices (330, 340) and the single-ported memory core 380. In one embodiment, the core frequency is twice that of the fastest port (310, 320) frequency. In this case, the multiplexing logic 370 may be enabled to "ping-pong" between serving the two ports (310, 320). Of course, other well known time multiplexing techniques could be employed for the other port frequencies.

In one embodiment, in the event that ports 310, 320 receive data simultaneously on the respective port data buses 312, 322, a controller 390 informs port multiplexing logic 370 which port data bus (312, 322) to receive data from first. For example, control signals 358 and 368 are for setting up the port multiplexing logic 370 through the controller 390. In yet another embodiment, as described above controller 390 may flip flop between receiving data from the port data lines 312, 322.

In yet another embodiment, the port synchronization logic devices (330, 340) synchronizes the information communicated between the ports (310, 320) and the single-ported memory core 380 by synchronizing the information between clocks associated with the ports (referred to hereinafter as "port clocks") and a clock associated with the single-ported memory core 380 (referred to hereinafter as a "core clock").

The device 300 may also include data read buses (352, 362) for communicating data from port multiplexing logic 370 to port synchronization logic devices (330, 340), data write buses (354, 364) for communicating data from port synchronization logic devices (330, 340) to port multiplexing logic 370, as well as address buses (356, 366) for communicating the address to port multiplexing logic 370 that the data from data write buses (354, 364) may ultimately be stored at in the single-ported memory core 380, according to another embodiment.

According to one embodiment, the bandwidth of address and data bus 372 for communicating between the port multiplexing logic 370 and the single-ported memory core 380 is at least the bandwidth of the combination of a first set of buses (352, 354, 356) and a second set of buses (362, 364, 366) for communicating between port synchronization logic devices (330, 340) and port multiplexing logic 370. In yet another embodiment, the bandwidth of address and data bus 372 for communicating between the port multiplexing logic 370 and the single-ported memory core 380 is at least twice the bandwidth of the highest of a first set of buses (352, 354, 356) and a second set of buses (362, 364, 366) for communicating between port synchronization logic devices (330, 340) and port multiplexing logic 370.

For at least the reasons discussed herein, the device 300 may be constructed with a single-ported memory core 380 to provide dual-ported functionality for multiple clock domains, which allows for random accesses as well as bi-directional data flow. In the case of device 300, the multiple clock domains are for the clocks associated with the ports 330, 340 and the single-ported memory core 380, according to one embodiment. The internal operation of the single-ported memory core 380 is

transparent to a user, thus, the dual-ported device 300 allows concurrent read and/or write operations on each port (330, 340) in the multiple clock domains.

FIG. 4 depicts a port synchronization logic device, e.g., device 330, according to one embodiment of the present invention. According to one embodiment, a port synchronization logic device may use FIFOs to synchronize information that is received and outputted. For example, the port synchronization logic device 440 includes a read data and control FIFO 442 for synchronizing data that is outputted, a write data and control FIFO 444 for synchronizing information that is received, and an address FIFO 446 for synchronizing addresses that are received. Typically, data and addresses are received and supplied at the port side according to the port clock rate, however, data and addresses on bus 454 and 456, as well as, data on bus 452 are at the core frequency.

According to one embodiment, data flows through device 440 in a bidirectional manner. For example, the port synchronization logic device 440 receives data from port 410's data bus 412 which it may communicate to a multiplexer, such as port multiplexing logic 370 depicted in FIG. 3, over a data write bus 454. In one embodiment, control signal 458 is for setting up a multiplexer, such as port multiplexing logic 370, through a controller, such as the controller 390. Ultimately the multiplexer 370 may communicate the received data to a single-ported memory core, such as single-ported memory core 380 depicted in FIG. 3 at the core frequency. Similarly, the port synchronization logic device 440 receives data from a single-ported memory core which it communicates to port 410's data bus 412 in data read mode.

In one embodiment, for a data read operation, an address is supplied from port 410 over bus 414 to FIFO 448, over bus 456 and the data supplied from core

380 is provided over bus 452 to FIFO 442 and to port bus 412. For a data write operation, addresses and data are supplied over buses 414 to FIFO 448 supplying data and addresses respectively over busses 454 and 456 to the core 380.

According to another embodiment, the bus 414 that addresses are received on is unidirectional. For example, when data is received on port data bus 412 the data may be ultimately stored on single-ported memory core 380 at the address received on port address bus 414.

In yet another embodiment, the FIFO's (442, 444, 446) are implemented with memory and/or synchronization registers. According to one embodiment, the read data and control FIFO 442 is only for receiving data from the data read bus 452. Similarly, according to one embodiment, the write data and control FIFO 444 is only for writing data to the data write bus 454.

Just as port clocks may be associated with ports 310, 320 in FIG. 3, a port clock may be associated with port 410 depicted in FIG. 4, according to one embodiment. According to another embodiment, the FIFO's (442, 444, 446) are used for synchronizing signals that cross the clock boundary between port 410 and a single-ported memory core. For example, when the port synchronization logic device 440 receives data from port 410 which it ultimately communicates to a single-ported memory core, write data and control FIFO 446 may synchronize the data from port 410's clock to the single-ported memory core's clock (referred to hereinafter as a "core clock"). The data may then be processed with respect to the core clock. Similarly, when the port synchronization logic device 440 receives addresses from port address bus 414, the address FIFO 446 may synchronize the addresses from port 410's clock to the core clock. Further, when the port synchronization logic device 440 receives

data from a single-ported memory core which it communicates to port 410, the read data and control FIFO 442 may synchronize the data from the core's clock to port 410's clock.

FIG. 5 depicts a port synchronization logic device according to one embodiment of the present invention. The port synchronization logic device 540, as depicted in FIG. 5, is similar to port synchronization logic device 440, depicted in FIG. 4, except that device 540 optimizes for the situation where port 410's clock is half as fast as the core clock by using multiplexers (542, 544, 546) to bypass the FIFO's (442, 446, 448). This embodiment may be used when the port clocks and the core clock are generated from the same clock circuit. For example, if port 410's clock is from the same source as the core clock, then data from the buses (452, 412, 414) would flow to the respective multiplexers (542, 544, 546). However, if port 410's clock is not from the same source as the core clock, then data from the control lines (452, 412, 414) would flow to the FIFOs (442, 440, 446). According to one embodiment, signal control lines (not shown) for each multiplexer (542, 544, 546) select whether or not to bypass the FIFOs (442, 446, 448). These lines may be enabled via configuration states.

According to another embodiment, devices, such as devices 300, 440, and 540, could be implemented on a monolithic substrate for example a single "chip," or on multiple monolithic substrates on a board such as a PCB or in a package such as a multi-chip module. According to one embodiment, devices, such as devices 300, 440, and 540, could also be implemented as programmable logic circuitry, for example, on a field programmable gate array (FPGA) or a complex programmable logic device (CPLD), or on a mask\programmable gate array.

Various embodiments of the present invention use a single-ported memory, thus, allowing a smaller and more economical die size for a smaller density than the conventional dual-ported memories. A designer can develop a controller that can be reused over technologies, and eliminates the cost of developing a dedicated dual-ported memory. This invention also enables a designer and/or vendor of dual-ported memories to, among other things, fill out a product portfolio to allow lower cost points, and also to scale up to larger port counts.

It should be appreciated that reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Therefore, it is emphasized and should be appreciated that two or more references to "an embodiment" or "one embodiment" or "an alternative embodiment" in various portions of this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures or characteristics may be combined as suitable in one or more embodiments of the invention.

Similarly, it should be appreciated that in the foregoing description of exemplary embodiments of the invention, various features of the invention are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed invention requires more features than re expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims following the detailed description are hereby expressly incorporated into

this detailed description, with each claim standing on its own as a separate embodiment of this invention.

The foregoing descriptions of specific embodiments of the present invention, a method and system for providing the functionality of dual-ported memory using single-ported memory thereby dual port operations can be emulated for applications operating according to different clock domains in a cost effective way, have been presented for purpose of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.